AN INTEGRATED HIGH-SPEED SERIAL-TO-PARALLEL AND PARALLEL-TO-SERIAL TRANSCEIVER

ABSTRACT OF THE DISCLOSURE

A transceiver includes a receiver section and a transmitter section. The receiver section includes a clocking circuit, a serial-to-parallel module, and compensation. The transmitter section includes a clocking circuit, parallel-to-serial module, and compensation. The compensation within the receiver section and transmitter section compensates for integrated circuit (IC) processing limits and/or integrated circuit (IC) fabrication limits within the clocking circuits, serial-to-parallel module, and parallel-to-serial module that would otherwise limit the speed at which the transceiver could transport data.